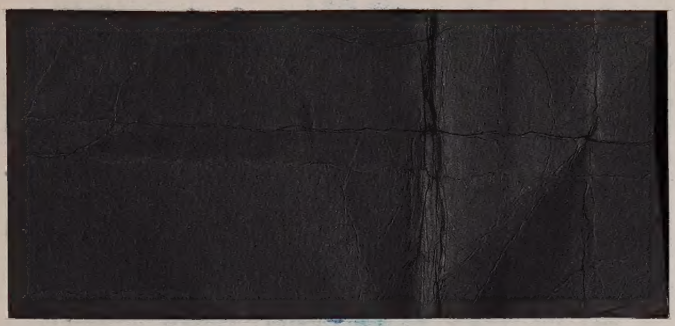
ME-7166
Vol. 2

tau-tron inc



ME-1A (7707-12)

ME-7166
Vol. 2

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ME7166

ME-1A

PSEUDORANDOM DATA
RATE MODIFIER
INSTRUCTION MANUAL

VOL 2 of 5

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INTRODUCTION

Tau-Tron Model ME-1A Pseudorandom Data Rate Modifier module is a cost effective method of increasing the frequency range of pseudorandom BERT (bit error rate test) systems. BERT systems operating up to 75 MHz maximum frequency can be extended to effectively operate to 150 MHz maximum frequency.

While any Tau-Tron pseudorandom generator/BERT receiver system with compatible pseudorandom sequences can be frequency range extended using ME-1A; the MN-1 Pseudorandom Data Generator and the MB-1 Error Rate Measurement Receiver are the ideal companion units. MN-1 and MB-1 provide a versatile BERT system covering the frequency range from less than 1 Hz to 75 MHz. With ME-1A, this BERT system can cover the range from less than 1 Hz to 150 MHz.

The ME-1A version differs from the normal ME-1 in that compensation has been added to the internal clock distribution so that the data rate multiplier section clock/data phasing will remain constant while the user slews the input clock frequency. Otherwise, the functions of the two versions of the ME-1 are identical.

SPECIFICATIONS

All inputs/outputs are at standard TMI signal levels as defined below.

INPUTS

CLOCK IN (f)---From less than 1 Hz to 150 MHz. Minimum pulse width is 3 ns. A sinewave may be used between 100 KHz and 150 MHz; typical trigger level is 2-3 volts peak-to-peak.

DX IN (f/2)---Transmit data pattern, NRZ format. Bit rate from less than 1 Hz to 75 MHz.

DR IN (f)---Receive data pattern, NRZ format. Bit rate from less than 1 Hz to 150 MHz.

OUTPUTS

CL 1 OUT (f/2)---Clock output for pseudorandom data generator at one-half the CLOCK IN frequency.

CL 2 OUT---Clock output for BERT receiver at full, one-half, or one-quarter the CLOCK IN frequency.

DB OUTPUT---Transmit data pattern, NRZ format. Bit rate from less than 1 Hz to 150 MHz.

DSØ1 OUTPUT---Receive data pattern, NRZ format. Bit rate from less than 1 Hz to 150 MHz.

DSØ2 OUTPUT---Receive data pattern, NRZ format. Bit rate from less than 1 Hz to 75 MHz.

CONTROLS

CODE LENGTH---Seven maximum-length pseudorandom sequence lengths are compatible: 6, 7, 9, 11, 15, 17, and 20. (Numbers indicate number of stages in generator shift register.)

PHASE DELAY---Individual controls for transmit and receive data inputs. Four phase delay positions (0, 1, 2, and 5 ns) for proper clock/data phase alignment.

MULTIPLIER OUTPUT FORMAT---Selects true/complement transmit data output.

MULTIPLIER RATE---Selects doubled (f) or undoubled (f/2) transmit data bit rate.

DIVIDER RATE---Selects unsampled (f), or one-half sampled (f/2), or one-quarter sampled (f/4) DSØ1 receive data bit rates. DSØ2 receive data bit rate is always one-half sampled (f/2).

INDICATORS

CLOCK IN ON---Clock input circuit is triggering properly.

LCHD---Data Latched (LCHD) indicators for transmit and receive data inputs; indicates proper clock/data phase relationship.

STANDARD TMI SIGNALS

LOGICAL ZERO---Between -200 mv and +600 mv.

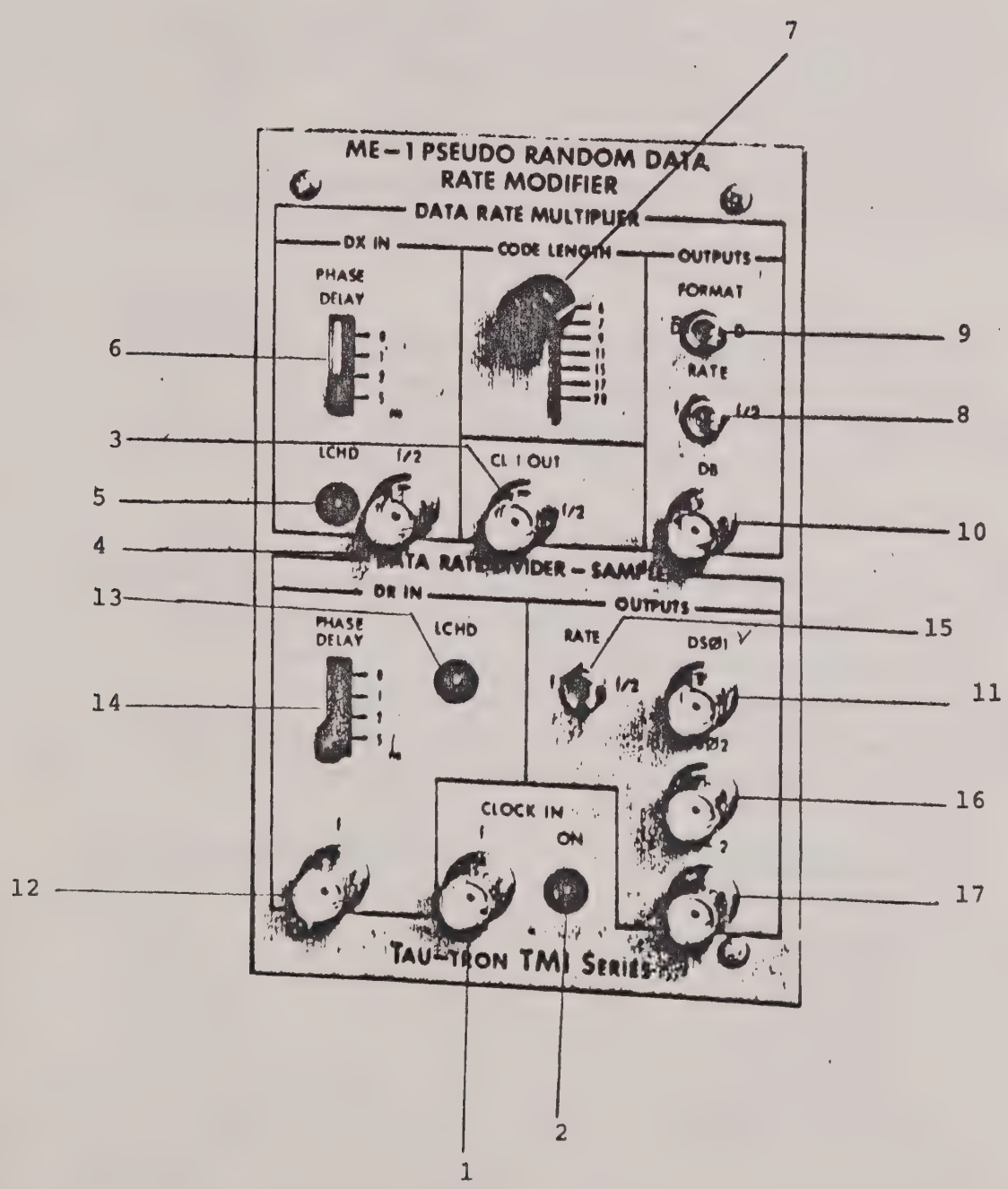
LOGICAL ONE---More positive than 1.7 volts.

STANDARD AMPLITUDE---2.0 volts typical.

TRANSITION EDGES---Typically 2 ns, 3.5 ns maximum.

IMPEDANCE---50 ohms to system ground.

WAVESHAPE DISTORTION---Less than ±7%, terminated.


ME-1 PSEUDO RANDOM DATA
RATE MODIFIER
DATA RATE MULTIPLIER
DX IN
CODE LENGTH
OUTPUTS
PHASE
DELAY
FORMAT
RATE
LCHD
1/2
CL I OUT
DB
DATA RATE DIVIDER - SAMPLE
DR IN
OUTPUTS
PHASE
DELAY
LCHD
RATE
DSØI
CLOCK IN
ON
TAU-TRON TMI SERIES
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17

OPERATING INSTRUCTIONS

Model ME-1 Pseudorandom Data Rate Modifier module consists of two functionally independent sections: a data rate multiplier, and a data rate divider. The single master clock input is shared between both sections; all other inputs/outputs and controls are independent. In the following description, numbers in parenthesis refer to the front panel diagram.

MASTER CLOCK INPUT

A single input clock (1) drives both the multiplier and divider sections. This clock must be at the desired data rate frequency (f) for the system under test. When sufficient clock levels exist to trigger the internal logic, the ON (2) LED will light.

MULTIPLIER SECTION

This section of the module will double the data rate of the pseudo-random data generator. Since the algorithm for producing double-rate sequences is dependent on the shift register length of the original maximum length sequence, only selected sequences can be doubled. In the ME-1A a wide selection of compatible sequences may be used: seven shift register lengths as given below:

SHIFT REGISTER LENGTH	CODE (SEQUENCE) LENGTH
6	63 bits
7	127 bits
9	511 bits
11	2,047 bits
15	32,767 bits
17	131,071 bits
20	1,048,575 bits

Figure 1 shows a typical transmitter configuration. The simple steps below will set up the ME-1 multiplier section:

1. Connect CL 1 OUT (3) to the pseudorandom data generator (MN-1) clock input.
2. Connect the pseudorandom data generator data output to DX IN f/2 (4).

3. The LCHD (5) (data latched) indicator will light if the clock/data phase is correct. If not, adjust the PHASE DELAY (6) until LCHD (5) lights.
4. Select the same CODE LENGTH (7) as is selected at the pseudorandom generator.
5. Select the output data RATE (8) as desired:
   f - double the input data rate.
   f/2 - same as the input data rate.
6. Select the true (D) or complementary ($\overline{D}$) output data format (9) as required.
7. The rate multiplied data is available at the DB (10) output.

Note that it is not necessary to disconnect the ME-1 when low frequency testing at the pseudorandom generator frequencies is desired.

DIVIDER SECTION

This section of the module will sample (divide) the double-rate data, and produce data rate outputs at frequencies compatible to the BERT receiver. During the sampling operation, two identical (except for a time shift) pseudorandom sequences are produced. Each represents a 180° phase shift from the other. Either one may be connected to the BERT receiver for error rate measurement. The measurement produced is the average error rate based on one-half of the received data. In most practical situations the error rate should be the same for either phase or the combined error rate. For cumulative error counting, as well as for simultaneous combined error rate measurement, both phases will have to be monitored.

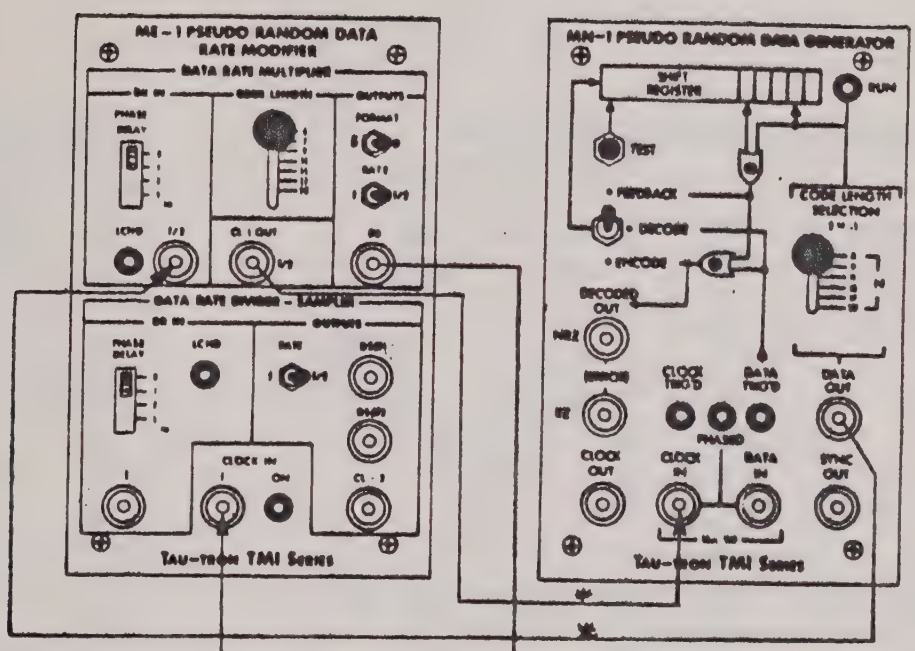
An auxilliary feature is the availability of a one-quarter rate output from DSØ1 (11). This represents one of four phases which result from an every fourth bit sampling of the received data. In some applications this additional information may be useful.

Figure 2 shows a typical receiver configuration. The simple steps below will set up the ME-1A divider section:

1. Connect the received data from the system under test to DR IN f (12).

2. The LCHD (13) (data latched) indicator will light if the clock/data phase is correct. If not, adjust the PHASE DELAY (14) until LCHD (13) lights.
3. Select the sampled data RATE (15) desired from DSØ1 (11):
   f - same as the received input data rate.
   f/2 - one-half the received input data rate.
   f/4 - one-quarter the received input data rate.
   (This is the unmarked center position of the switch.)
4. The selected sampled data rate output is available at DSØ1 (11) for use by the BERT receiver (MB-1) data input. A one-half data rate output is always available at DSØ2 (16). DSØ1 and DSØ2 are 180° out of phase when f/2 is selected in step 3.
5. A clock output (17) at the selected frequency (per step 3) is available for use by the BERT receiver clock input.

Note that it is not necessary to disconnect the ME-1A when performing low frequency testing at received data input rates compatible with the BERT receiver. By selected the f rate in step 3 above a true bit-by-bit (unsampled) error rate measurement can be made.



From Signal Source (e.g. MS-2)

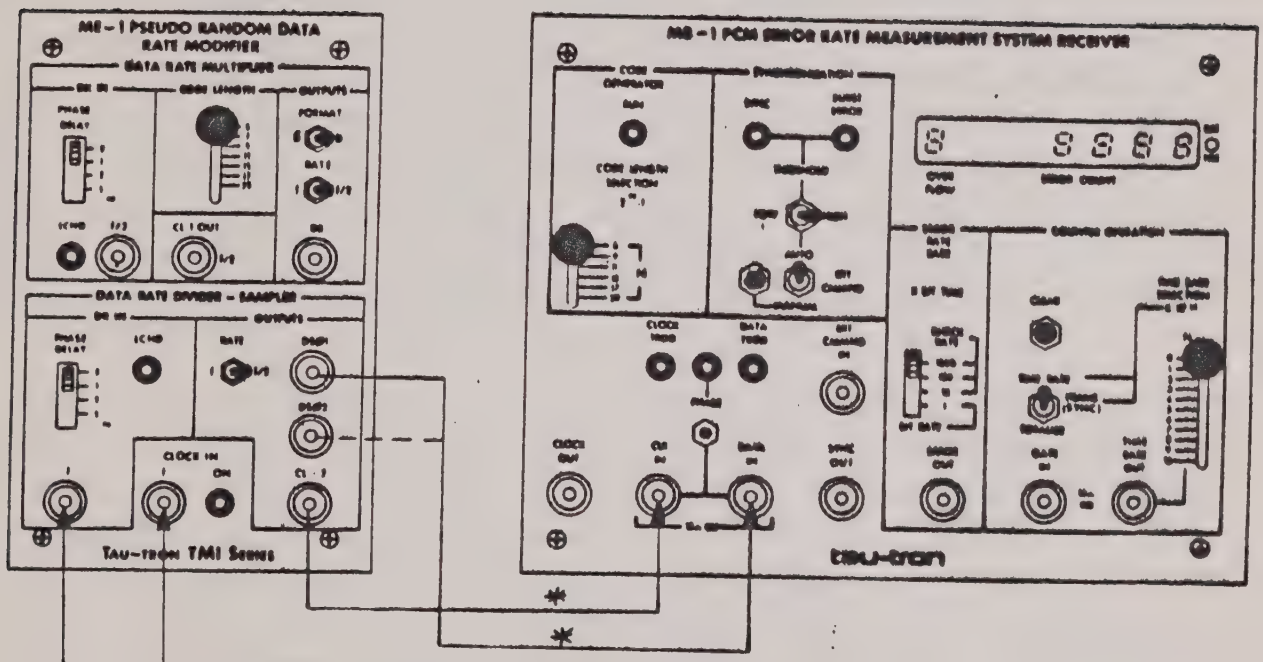
Multiplied Data To System Under Test.

NOTE: All connections shown are 50 ohm coax cables.

* The MN-1 clock/data cables must total 7 ns (56 in of RG-58) length in order to be able to sweep through the frequency range without re-adjusting delays.

TYPICAL TRANSMITTER CONFIGURATION

FIGURE 1


ME-1 PSEUDO RANDOM DATA RATE MODIFIER
DATA RATE MULTIPLIER
DATA RATE DIVIDER - SAMPLER
CLOCK IN
TAU-TRON TMI Series
ME-1 PCM ERROR RATE MEASUREMENT SYSTEM RECEIVER
From Signal Source (e.g. MS-2)
Data Received from System Under Test
* Clock/data cable lenghts per MB-1 instruction manual (typ. data cable longer than clock).

NOTE: All connections shown are 50 ohm coax cables

TYPICAL RECEIVER CONFIGURATION
FIGURE 2

TIMING CONSIDERATIONS

MULTIPLIER SECTION

The ME-1A has internal clock distribution compensation to enable it to hold DX IN F/2 (4) clock/data skew throughout the frequency range, if set up properly. When using at one fixed frequency the cable length restrictions below need not be followed; however, DX IN PHASE DELAY(6) may have to be readjusted if the frequency is changed. The delay from CL1 OUT (3) to the MN-1 and back to DX IN F/2 (4) of the ME-1A forms a critical path. In order for the clock and data to remain in constant phase alignment, this external path is matched internally by a clock delay line. This restricts the total cable delays to 7 ns; e.g. 3.5 ns each cable or any other combination equalling 7 ns. Using 8 in per ns for RG-58, this allows a total of 56 in of cable. Steps 1 and 2 on p.5 must meet the above cable length restriction. Normally the adjustment in step 3 will result in either 1 ns or 2 ns selected by the PHASE DELAY (6).

Two choices are available for output clock. The first is to use a spare clock output from the signal source (e.g. MS-2); but this will require a long delay cable to de-skew clock and data over the frequency range. A second alternative is to use the CL2 (17) output of the divider section; providing the system-under-test is half duplex. Be sure to select the same clock rate (15) as the data rate selection (8).
Typical skew between data output (10) and CL2 output (17) is clock leading data by 2 to 2.5 ns.

DIVIDER SECTION

The divider section has been compensated in its data input path by the amount of delay necessary to compensate the internal clock for multiplier clock slew operation, as described above. For slewing across the frequency range the ideal input timing is clock in (1) leading data in (12) by 2 to 2.5 ns.

Divider section clock output (17) will typically lead DSØ1 (11) by 1 ns. When the divider is in f/2 mode (15), the clock output (17) typically leads DSØ2 (16) by 2 ns. The cables from the ME-1 to the MB-1 (or MB-1A) must be adjusted according to the required clock/data phase relationship described in the MB-1 (MB-1A) manual. Typically this requires a longer clock cable than data cable.

THEORY OF OPERATION

ME-1A operates on two basic principles of pseudorandom sequences. The first principle is that the modulo-2 addition of two identical, but out of phase, pseudorandom sequences will produce a third identical pseudorandom sequence which is out of phase with the first two sequences. The second principle is that if two identical pseudorandom sequences which are 180° out of phase are sampled alternately by a double frequency clock, the result will be an identical pseudorandom sequence at twice the bit rate of the original sequences. Conversely, sampling a pseudorandom sequence at one-half the bit rate will produce two identical pseudorandom sequences 180° out of phase.

These principles are well discussed in the literature and will not be proved in this text.

INPUT CIRCUITS

Both transmit data (DX IN) and receive data (DR IN) are handled the same way. They are converted to ECL levels and the passed through a gate delay chain. Various points along the chain, including the input point, are brought to a multiplexer circuit which selects the appropriately delayed data signal under front panel control.

The data latched (LCHD) circuit consists of a flip-flop which is clocked true by data transitions and reset by differentiated clock pulses. The output of this detector latch drives a toggle mode flip-flop, which drives a capacitively coupled LED driver amplifier.

The clock input is converted to ECL, differentiated, and divided by 2. Full frequency and half frequency clocks are distributed to appropriate logic elements. The half-frequency clock also drives a capacitively coupled LED driver amplifier to indicated clock triggered properly.

MULTIPLIER CIRCUIT

The multiplier circuit consists of a 12 stage shift register, three multiplexers, exclusive-or and sampling logic. For each sequence (code) length selection, three different shift register taps are selected, producing three out of phase, identical pseudo-random sequences. Two of the sequences are modulo-2 added by the exclusive-or function, using the first principle above, to produce a sequence which is 180° out of phase with the third shift register tap.

In multiply (RATE = f) mode, the two 180° apart sequences are alternately sampled by the clock input frequency, using the second principle above, to produce a double-rate pseudorandom sequence, identical to the input sequence. When multiply is not selected (RATE = f/2), the sampling logic is disabled, and the third shift register tap passed through to the output amplifier.

DIVIDER CIRCUIT

The divider circuit consists of a divide-by-4 counter, multiplexer, and two sampling flip-flops. The divide-by-4 counter is used to produce both phases of half frequency clock, and one phase of one-quarter frequency clock.

Both sampling flip-flops operate identically. Full rate data is applied to both flip-flops. The appropriate clock is used to produce the desired sampled data. A multiplexer selects either full frequency, half frequency, or quarter frequency clocks to produce full rate (f), half rate (f/2) or quarter rate (f/4) data at DSØ1. The 180° phased half frequency clock is always applied to the DSØ2 sampling flip-flop.

OUTPUT CIRCUITS

Multiplier output data is resynchronized by the appropriate clock (either full or half frequency) and converted to standard TMI levels. A half frequency clock (f/2) is converted to TMI levels to drive the pseudorandom data generator.

The outputs of the sampling flip-flops in the divider section are converted to standard TMI levels. A clock amplifier converts the DSØ1 sample clock to TMI levels.

MULTIPLIER CLOCK/DATA SKEW

The clock path from the point at which CL1 OUT is generated to the multiplier shift register input is delayed to compensate for the data path internal/external cable delays and for the MN-1 insertion delay. Two delay lines are used to accomplish this: one delays full frequency clock, while the other delays half frequency clock.

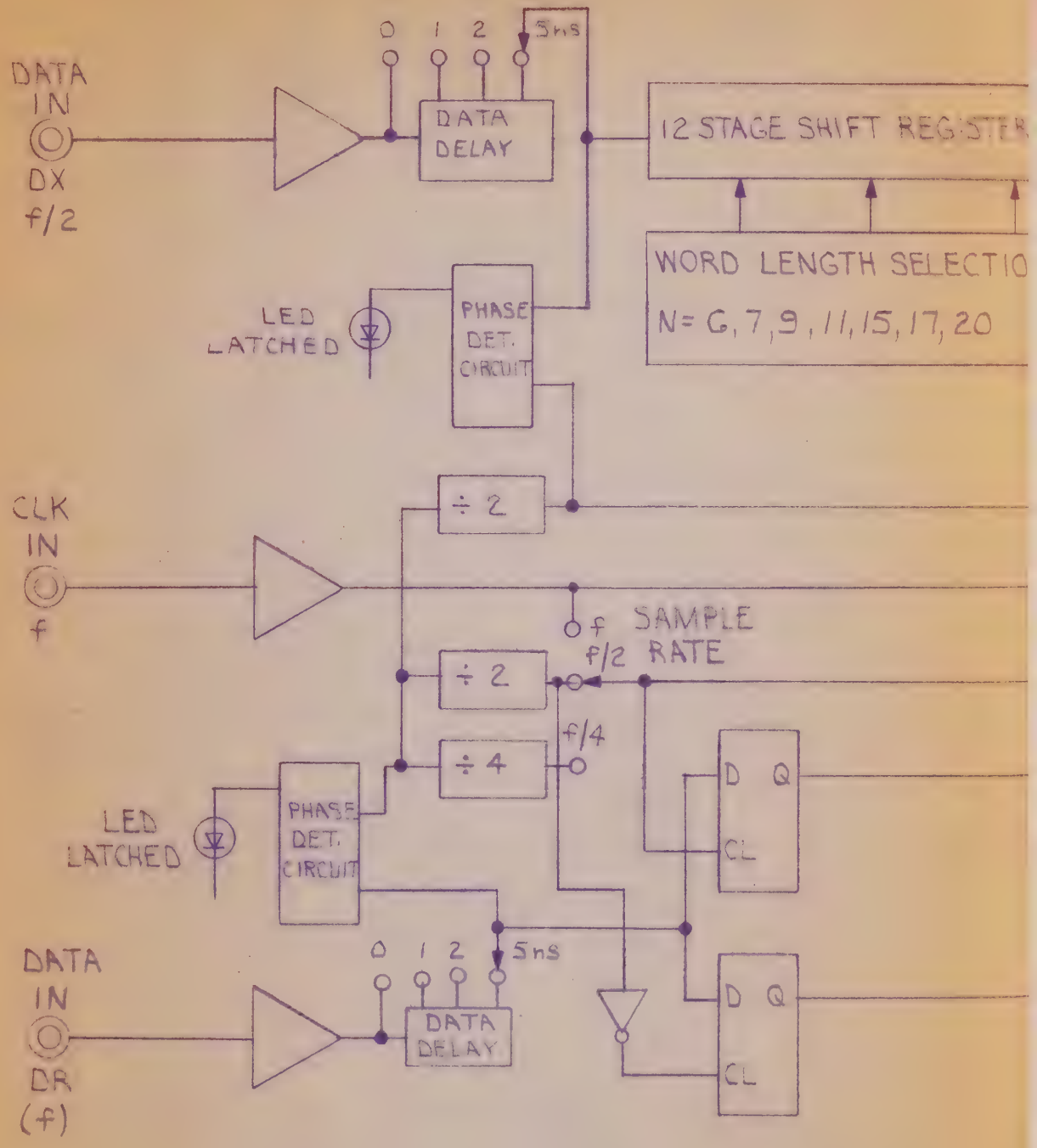
In the receiver section, a third delay line is used to restore the input clock/data phase relationship as normally found in ME-1.

LIST OF ILLUSTRATIONS

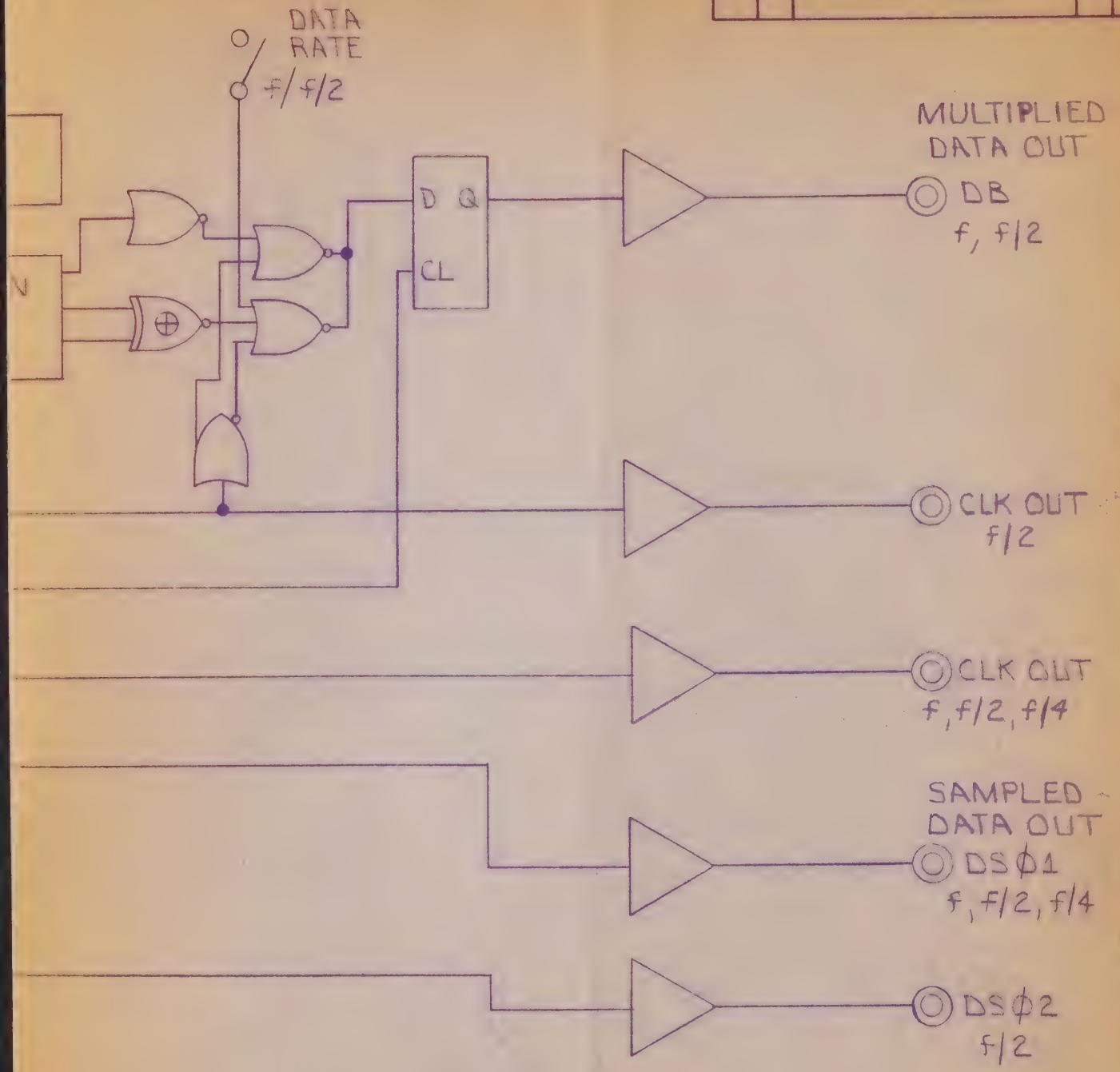
ME-1A Block Diagram----------TBN-53396

Data Rate Extender with
Clock Skew Provision Schematic----------TDJ-54036

Module Power Supply----------TAJ-53383


DATA IN
DX
f/2
0 1 2 5ns
DATA DELAY
12 STAGE SHIFT REGISTER
WORD LENGTH SELECTIO
N= 6, 7, 9, 11, 15, 17, 20
LED LATCHED
PHASE DET. CIRCUIT
CLK IN
f
÷ 2
÷ 2
÷ 4
f SAMPLE RATE
f/2 RATE
f/4
D Q
CL
LED LATCHED
PHASE DET. CIRCUIT
DATA IN
DR
(f)
0 1 2 5ns
DATA DELAY
D Q
CL

DATE	SYM	REVISION RECORD	DR	CK.



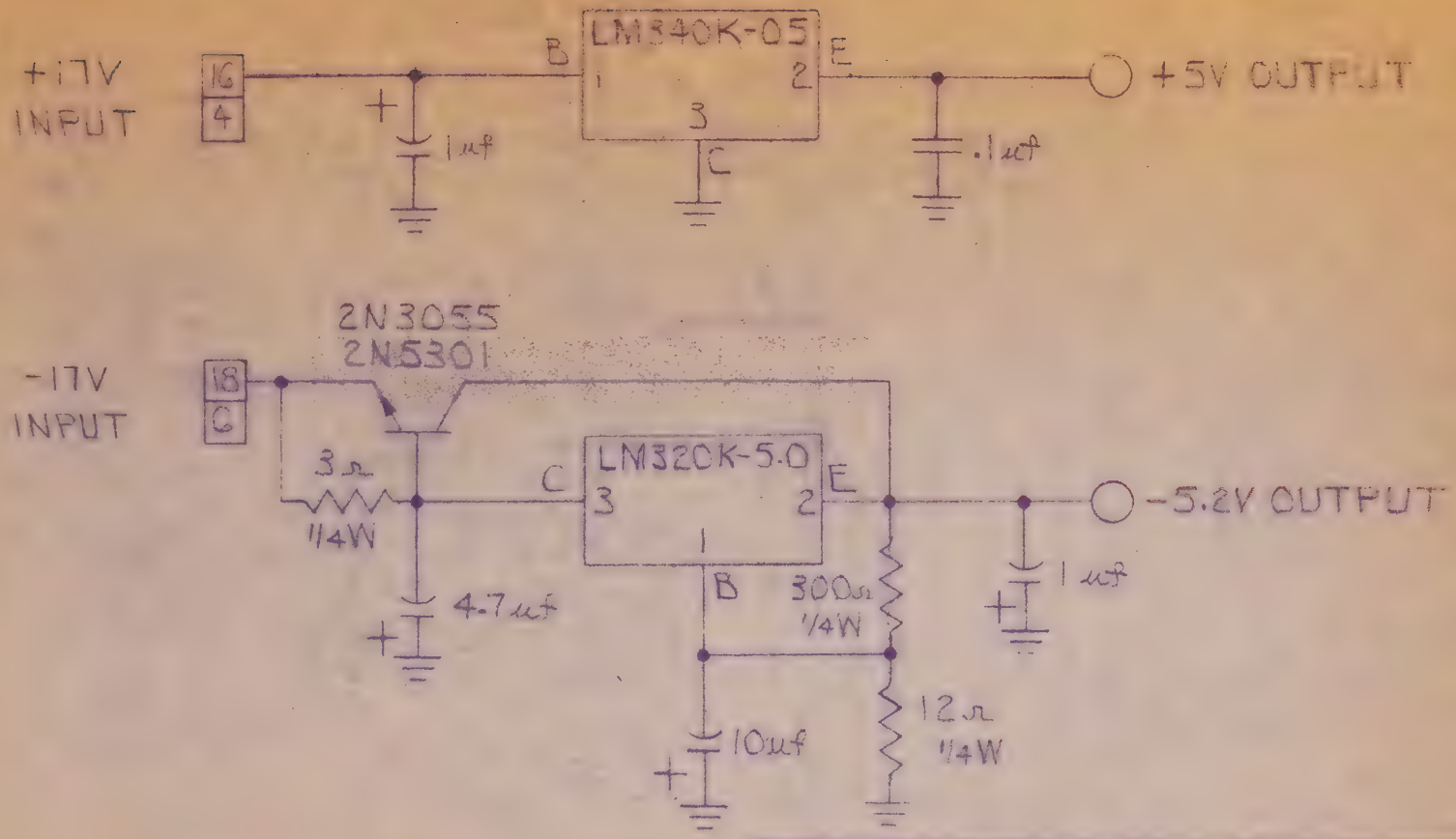
TOLERANCES (EXCEPT AS NOTED)	TAU-TRON INC		
DECIMAL ±	TMI SERIES	SCALE	DRAWN BY / APPROVED BY
FRACTIONAL ±	TITLE: ME-1 BIT RATE MODIFIER BLOCK DIAGRAM		
ANGULAR ±	DATE: 11-12-74	DRAWING NUMBER: TBN-53396	

DATE	BY	REVISION RECORD	DR	CK

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE VALUES ARE IN OHMS ±5% 1/8W
   b) CAPACITANCE VALUES ARE IN MICROFARADS
2. ⊣⊢ DENOTES 470Ω to -5.2V

TOLERANCES (EXCEPT AS NOTED)	TITLE: TELETYPE		
DECIMAL ±	TMI-SERIES	SCALE –	DRAWN BY EAC
FRACTIONAL ±	TITLE: ME-1A DATA RATE EXTENDER WITH CLOCK SLEW PROVISION		APPROVED BY
ANGULAR ±	DATE	DRAWING NUMBER: TDJ-54036	

DATE	SYM	REVISION RECORD	DR.	CK



TOLERANCES (EXCEPT AS NOTED)	TAU-TRON INC.		
DECIMAL ±	TMI SERIES	SCALE —	DRAWN BY J. P. Bartolucci APPROVED BY
FRACTIONAL ±	TITLE SCHEMATIC MODULE POWER SUPPLY (+5V, -5V BOOST)		
ANGULAR ±	DATE 11/5/74	DRAWING NUMBER TAJ-53383	

BRUNING 40-Z1

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WARRANTY

All Tau-Tron products are warranted against any defects in material and workmanship. This warranty applies for one year from the date of delivery for all Tau-Tron manufactured products. The warranty period for OEM products sold by Tau-Tron will depend on the original OEM warranty (consult factory for specific products). We will repair or replace products which, upon our examination, prove to be defective during the warranty period. NO OTHER WARRANTY, EXPRESSED OR IMPLIED, INCLUDING FITNESS FOR PURPOSE, MERCHANTIBILITY, OR OTHERWISE, IS GIVEN.

For any assistance, contact the factory and be prepared to provide Instrument Model and Serial Numbers and all details regarding the manfunction.

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